WHAT IS CLAIMED IS:

1. A path memory circuit for use in a Viterbi decoding process performed based on state transitions through a number n (n is a positive integer) of states, comprising M (M is a positive integer) stages of storage circuits, each storage circuit including n rows of selective storage circuits, each selective storage circuit including a selection circuit for selectively outputting an input according to a result of the Viterbi decoding and a storage element circuit for storing a result selectively outputted from the selection circuit, the path memory circuit comprising:

a memory area **A** formed by the storage circuits of the first to i^{th} (i is an integer from 0 to M) stages;

a memory area **B** formed by the selective storage circuits that select and hold a decoding result for any state k (k is an integer from 1 to n) of the storage circuits from the $i+1^{th}$ stage to the M^{th} stage; and

a memory area **C** formed by the selective storage circuits other than the memory area **A** and the memory area **B**,

wherein according to a memory length control signal, the storage circuits of the j (j is an integer from i+1 to M)th and subsequent stages in the memory area **C** are stopped, and the selection circuits of the j^{th} and subsequent stages in the memory area **B** select an output of the selective storage circuits of a preceding storage circuit belonging to the memory area **B**.

2. The path memory circuit of claim 1, further comprising:

memory length setting means for setting, to a first state, the memory length control signal to the storage circuit of a stage so as to set a path memory length to an intended length depending on a status of a signal to be Viterbi-decoded; and

logical sum means for, when the memory length control signal to the storage circuit of a stage is set to the first state, setting, to the first state, the memory length control

signal to the storage circuit of the following stage.

3. The path memory circuit of claim 1, further comprising:

convergence determination means for, when it is determined that outputs from all the storage element circuits of a stage are equal to one another, setting, to a first state, the memory length control signal to the storage circuit of the following stage; and

logical sum means for, when the memory length control signal to the storage circuit of a stage is set to the first state, setting, to the first state, the memory length control signal to the storage circuit of the following stage.

4. The path memory circuit of claim 1, wherein when the storage circuits of the j^{th} and subsequent stages in the memory area **C** are stopped according to the memory length control signal, each of the storage element circuits of the j^{th} and subsequent stages in the memory area **B** outputs its input signal as it is, irrespective of a clock signal.

5. The path memory circuit of claim 4, wherein the storage element circuit in the memory area **B** includes:

data holding means for taking in an input signal when a synchronization pulse signal is in a first state and for holding the input signal when the synchronization pulse signal is in a second state; and

synchronization pulse producing means, receiving a synchronization signal and a control signal as its inputs, for outputting the synchronization pulse signal in the first state when the control signal is in the first state and for producing a pulse signal from the synchronization signal and outputting the produced pulse signal as the synchronization pulse signal when the control signal is in the second state,

wherein the memory length control signal is used as the control signal of the synchronization pulse producing means.

6. The path memory circuit of claim 4, wherein the storage element circuit in the memory area **B** includes:

master storage means for holding an input signal when a first synchronization signal is in a first state and for taking in the input signal when the first synchronization signal is in a second state;

slave storage means for taking in an output of the master storage means when a second synchronization signal is in the first state and for holding the output when the second synchronization signal is in the second state; and

synchronization signal producing means, receiving a synchronization signal and a control signal as its inputs, for outputting the synchronization signal as the first synchronization signal, for outputting an inverted version of the synchronization signal as the second synchronization signal when the control signal is in the first state, and for outputting the synchronization signal as it is as the second synchronization signal when the control signal is in the second state,

wherein the memory length control signal is used as the control signal of the synchronization signal producing means.

7. The path memory circuit of claim 4, wherein each storage element circuit in the memory area **B** is a latch circuit, the path memory circuit further comprising:

synchronization pulse producing means for producing a pulse signal from a received synchronization signal and outputting the produced pulse signal; and

a driver circuit, receiving an output from the synchronization pulse producing means and the memory length control signal, for outputting a signal in a first state when the memory length control signal is in the first state, and for outputting an output from the synchronization pulse producing means when the memory length control signal is in the second state,

wherein an output signal from the driver circuit is given as a synchronization signal to the memory area **B**.

8. The path memory circuit of claim 1, wherein the memory area **B** includes:

a synchronous-type selective storage circuit for holding and outputting an input in synchronism with a clock signal when the memory length control signal is in a first state;

a repeater-type storage element circuit for outputting an input signal as it is, irrespective of the clock signal, when the memory length control signal is in the first state.

9. The path memory circuit of claim 1, wherein:

each storage element circuit in the memory area **B** includes a circuit for a scan test, and a scan path is formed by connecting together the storage element circuits in an order starting from the $i+1^{th}$ stage to the M^{th} stage; and

the storage element circuits of the j^{th} and subsequent stages in the memory area **B** operate in a scan test mode when the storage circuits of the j^{th} and subsequent stages in the memory area **C** are stopped according to the memory length control signal.

10. The path memory circuit of claim 1, wherein groups of circuit elements forming the memory area **A**, the memory area **B** and the memory area **C** are each placed in a single independent area, with the memory area **B** corresponding to a first row or an n^{th} row of the memory area **A** and being positioned next to that row of the memory area **A**.

11. The path memory circuit of claim 1, wherein the memory area **B** is formed by the selective storage circuits belonging to such a state that one input of the selection circuit is an output from the selective storage circuit of the same state for one time segment ago.

12. The path memory circuit of claim 1, wherein when the j^{th} and subsequent stages of the memory area **C** are stopped, a supply of a clock signal to the j^{th} and subsequent stages of the memory area **C** is stopped.

13. The path memory circuit of claim 12, wherein when the j^{th} and subsequent stages of the memory area **C** are stopped, a back bias is applied to a substrate of transistors included in the j^{th} and subsequent stages of the memory area **C**.

14. The path memory circuit of claim 1, wherein when the j^{th} and subsequent

stages of the memory area **C** are stopped, a power supply to the j^{th} and subsequent stages of the memory area **C** is stopped.